PI3B3253

3.3V, Dual 4:1 Mux/DeMux NanoSwitch™

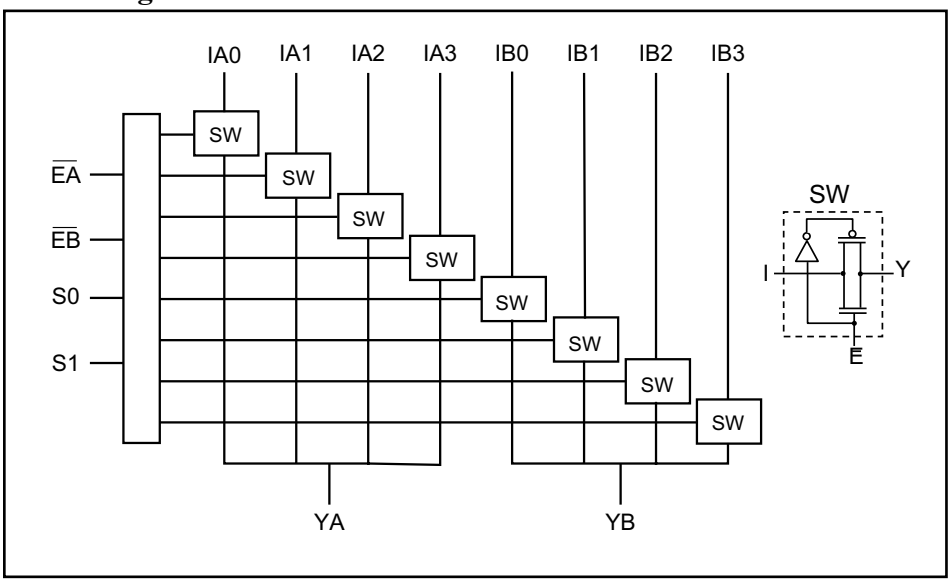
Features

- Near-Zero propagation delay
- 5Ω switches connect inputs to outputs
- Fast Switching Speed: 5.2ns max.
- Ultra Low Quiescent Power (0.2µA typical)
  – Ideally suited for notebook applications
- Pin compatible with 74 series 253 logic devices
- Packaging (Pb-free & Green available):
  – 16-pin 150-mil wide plastic QSOP (Q)
  – 16-pin 173-mil wide plastic TSSOP (L)
  – 16-pin 150-mil wide plastic SOIC (W)

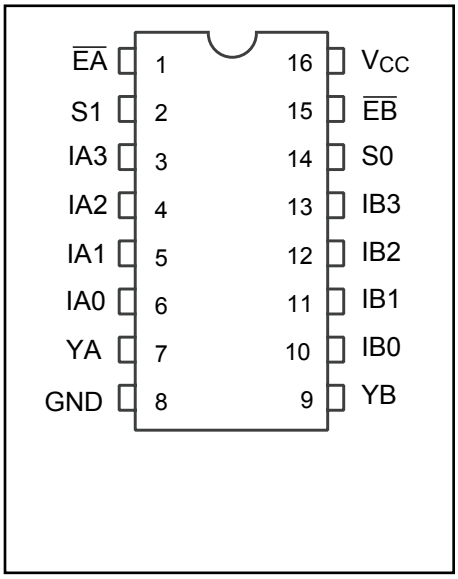
Description

The PI3B3253 is a 3.3V, Dual4:1 Multi-plexer/ Demultiplexer with Hi-Z outputs that is pinout compatible with the PI74FCT253T, 74F253, and 74ALS/AS/LS 253. Inputs can be connected to outputs with low On-Resistance (5Ω) with no additional ground bounce noise or propagation delay.

Block Diagram



Pin Configuration



Truth Table(1)

Enable		Select		Y_A	Y_B	Function
$\overline{E_A}$	$\overline{E_B}$	S_1	S_0			
H	X	X	X	Hi-Z	X	Disable A
X	H	X	X	X	Hi-Z	Disable B
L	L	L	L	$_IA_0$	$_IB_0$	S1-0 = 0
L	L	L	H	$_IA_1$	$_IB_1$	S1-0 = 1
L	L	H	L	$_IA_2$	$_IB_2$	S1-0 = 2
L	L	H	H	$_IA_3$	$_IB_3$	S1-0 = 3

Note:
1. H = High Voltage Level, L = Low Voltage Level

Pin Description

Pin Name	Description
$_IA_N$, $_IB_N$	Data Inputs
S_{0-1}	Select Inputs
$\overline{E}_A$, $\overline{E}_B$	Enable
Y_A, Y_B	Data Outputs
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential	–0.5V to +4.6V
DC Input Voltage	–0.5V to +4.6V
DC Output Current	120mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} =3.3V ±10%)

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	–0.5		0.8	
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			±1	
I_{OZH}	High Impedance Output Current	0 ≤ I_N, Y_N ≤ V_{CC}			±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA			–1.2	V
R_{ON}	Switch On-Resistance[3]	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 48mA or 64mA		5	8	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA		10	17	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between I and Y pin at indicated current through the switch. On-Resistance is determined by the lower of the voltages on the two (I,Y) pins.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[1]	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	3.0	pF
C_{OFF}	I_A/I_B Capacitance, Switch Off		8.0	
C_{ON}	I_A/I_B Capacitance, Switch On		36.0	

Notes:
1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	3.0	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.0V[3]			750	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (control inputs only); I and Y pins do not contribute to I_{CC}.

Switching Characteristics over Operating Range

Parameters	Description	Test Conditions	Com.		Units
			Min.	Max.	
t_{IY}	Propagation Delay[1,2] In to Yn	C_L = 50pF R_L = 500Ω		0.25	ns
t_{SY}	Bus Select Time, Sn to Yn		1	4.0	
t_{PZH}	Bus Enable Time, $\overline{E}$ to Yn		1	3.8	
t_{PHZ} t_{PLZ}	Bus Disable Time, $\overline{En}$ to Y		1	5.2	

Notes:
1. This parameter is guaranteed but not tested on Propagation Delays.
2. The bus switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Applications Information

Logic Inputs

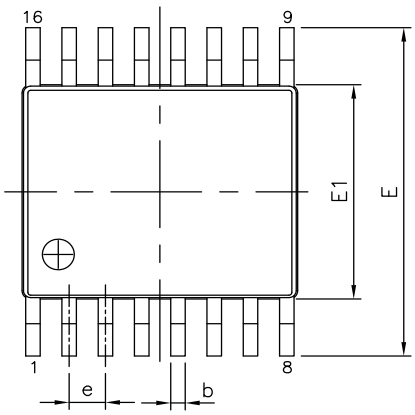
The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, IN may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

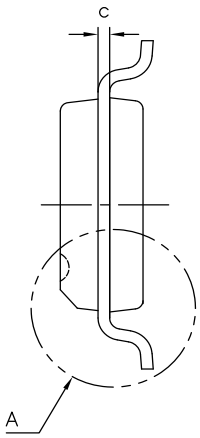
Power-Supply Sequencing and Hot Plug Information

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} and GND before applying signals to input/output or control pins.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

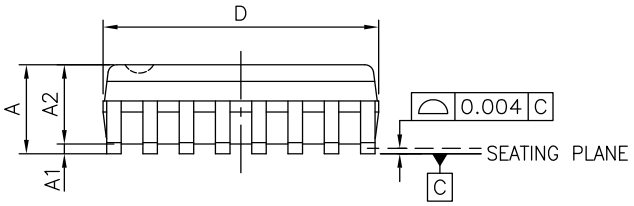
Packaging Mechanical: 16-Pin QSOP (Q)

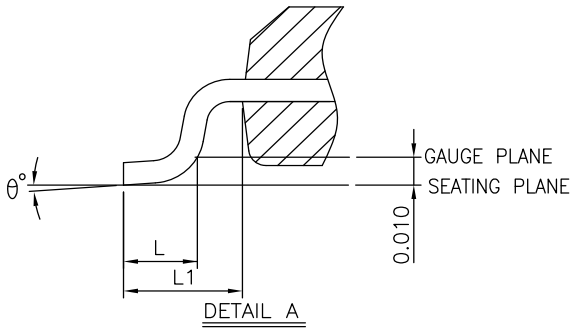




SYMBOLS	MIN.	NOM.	MAX.
A	—	—	0.069
A1	0.004	—	0.0098
A2	0.049	—	—
b	0.008	—	0.012
c	0.004	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.158
E	0.228	0.236	0.244
L	0.016	—	0.050
L1		0.041 REF.	
e		0.025 BSC.	
θ°	0	—	8

UNIT : INCH



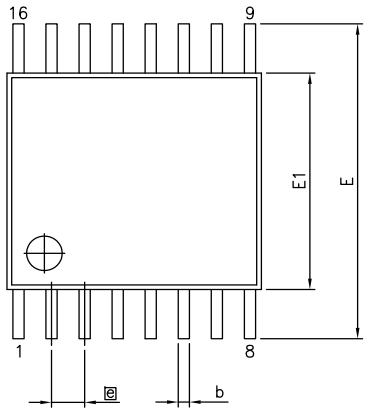


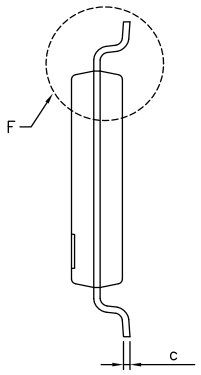
NOTES:
1. ALL DIMENSIONS IN INCH. ANGLES IN DEGREES.
2. JEDEC MO-137E
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity	DATE: 04/08/16
DESCRIPTION: 16-Pin, 150mil Wide QSOP	
PACKAGE CODE: Q (Q16)	
DOCUMENT CONTROL #: PD-1201	REVISION: H

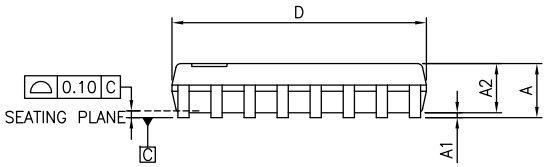
16-0056

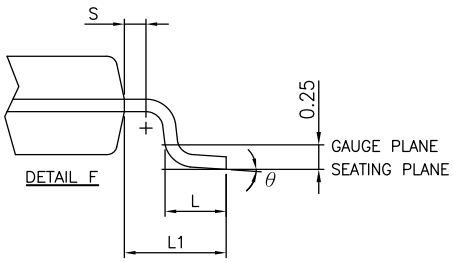
Packaging Mechanical: 16-Pin TSSOP (L)





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO-153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

DATE: 03/24/16

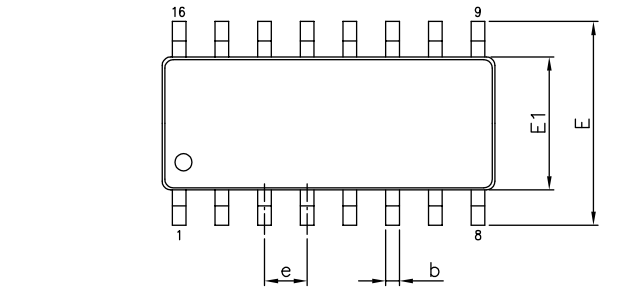
DESCRIPTION: 16-Pin, 173mil Wide TSSOP

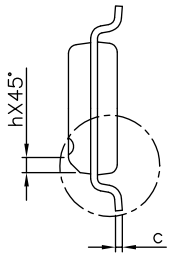
PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310 REVISION: G

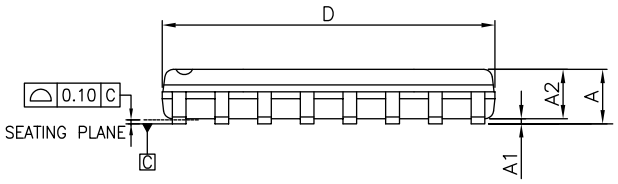
16-0061

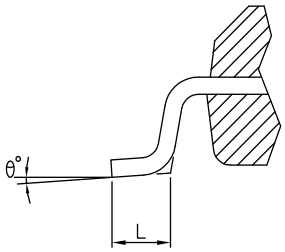
Packaging Mechanical: 16-Pin SOIC (W)





SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.00	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	9.80	9.90	10.0
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
L	0.40	–	1.27
h	0.15	–	0.50
θ°	0	–	8





NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC OUTLINE : MS-012 AC
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MIN. DIMENSION OF A2 AND h ARE OUT OF JEDEC SPEC.

DIODES INCORPORATED | PERICOM A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY

DATE: 06/30/16

DESCRIPTION: 16-Pin, 150mil Wide SOIC

PACKAGE CODE: W

DOCUMENT CONTROL #: PD-1004 REVISION: G

16-0145

Note: For latest package info, please check: http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Desciption
PI3B3253QE	Q	16-pin, 150mil Wide (QSOP)
PI3B3253QEX	Q	16-pin, 150mil Wide (QSOP), Tape & Reel
PI3B3253LE	L	16-pin, 173mil Wide (TSSOP)
PI3B3253LEX	L	16-pin, 173mil Wide (TSSOP), Tape & Reel
PI3B3253WE	W	16-pin, 150mil Wide (SOIC)
PI3B3253WEX	W	16-pin, 150mil Wide (SOIC), Tape & Reel

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel

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